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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,499	03/19/2004	Akiyoshi Aoyagi	9319S-000701	8386

27572 7590 09/30/2005

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EXAMINER	
KUNZER, BRIAN	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,499	AOYAGI, AKIYOSHI	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04, 7/29/04, 4/14/05, 5/31/05, 7/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-16 in the reply filed on September 20, 2005 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6, 7, 9, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Byun (6,736,306 B2).

3. With respect to claim 1, Byun teaches, from fig. 6, a semiconductor device comprising:

a first semiconductor package (120), in which a plurality of first joining points (124 and 170b) are formed, the first joining points including different areas for protruding electrodes; and

a second semiconductor package (150), in which a plurality of second joining points (154 and 180b) are formed, the second joining points including different areas for the protruding electrodes and being arranged so as to be opposed to the respective first joining points (124 and 170b).

4. With respect to claim 2, Byun teaches, from fig. 6 and fig. 8c, the said areas of each of the joining points (124 and 170b) are opening areas of an insulating layer (122) on lands (164) with which the protruding electrodes (160 and 162) are joined.

5. With respect to claim 3, Byun teaches, from fig. 5, the said areas of each of the joining points (124 and 170) are gradually changed from a central portion toward an outer peripheral portion of the semiconductor package (120).

6. With respect to claim 6, Byun teaches, from fig. 6, a semiconductor device, comprising:

a first semiconductor package (150); and

a second semiconductor package (120), stacked on the first semiconductor package (150) through a plurality of protruding electrodes (160 and 162) including different volumes.

7. With respect to claim 7, Byun teaches, from fig. 5, the volumes of the protruding electrodes (160 and 162) are gradually changed from a central portion toward an outer peripheral portion of the semiconductor packages.

8. With respect to claim 9, Byun teaches, from fig 8b, the said semiconductor device wherein each of the protruding electrodes has different amounts of conductive paste (168). (see column 5, lines 12-14)

9. With respect to claim 14, Byun teaches, from fig. 4-6, a semiconductor package, wherein areas of joining points of protruding electrodes joined with one package are changed corresponding to a warping of another package connected to the one package. (see column 2, lines 7-24)

10. With respect to claim 15, Byun teaches an electronic apparatus, comprising:

a first semiconductor package (C), in which a plurality of first joining points are formed, the first joining surfaces including different areas for protruding electrodes (3);

a second semiconductor package (B), in which a plurality of second joining points are formed, the second joining points including different areas for the protruding electrodes and being arranged so as to be opposed to the first joining points; and

a motherboard, on which the first semiconductor package is mounted. (See column 4, lines 43-47)

11. Claims 1, 5, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen (6,774,473 B1).

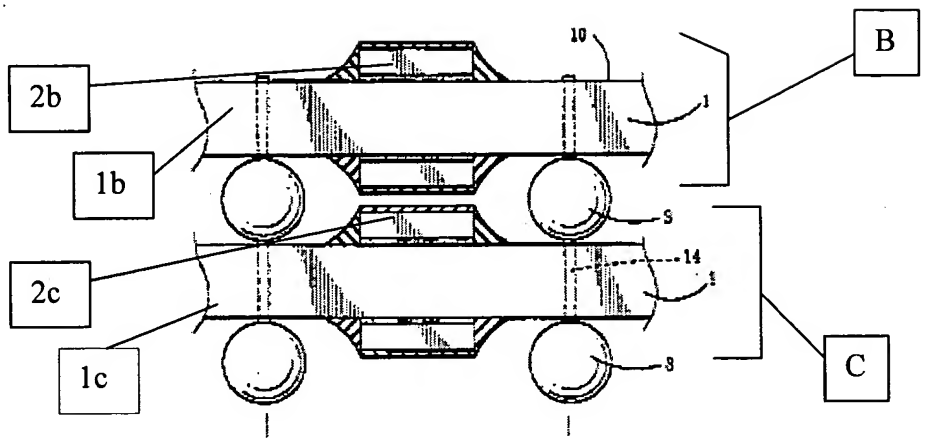

Figure A – A first semiconductor package (B) mounted on a second semiconductor package (C).

Reproduced from Shen (6,774,473 B1) – fig. 5.

12. With respect to claim 1, Shen teaches a semiconductor device (see figure A above) comprising:

a first semiconductor package (B), in which a plurality of first joining points (end of 14) are formed, the first joining points including different areas for protruding electrodes (3) (see also fig. 1); and

a second semiconductor package (C), in which a plurality of second joining points (other end of 14) are formed, the second joining points including different areas for the protruding electrodes and being arranged so as to be opposed to the respective first joining points. Note that the joining points include different areas on the substrate (1) for the electrodes (3).

13. With respect to claim 5, Shen teaches, from fig. 5, the said semiconductor device wherein volumes of the protruding electrodes (3) connected to each of the plurality of joining points (ends of 14) are substantially the same.

14. With respect to claim 10, Shen teaches the said semiconductor device wherein:

the first semiconductor package comprises (C):

a first carrier substrate (1c); and

a first semiconductor chip (2c), flip-chip mounted on the first carrier substrate (1c), and

the second semiconductor package (B), comprises:

a second carrier substrate (1b), mounted on the first carrier substrate (1c) through the protruding electrodes (3) so as to be held above the first semiconductor chip (2c);

a second semiconductor chip (2b), mounted on the second carrier substrate (1b); and

a sealing material (23, see fig 1) sealing the second semiconductor chip (2b). (See figure A above and fig. 1 of Shen)

15. With respect to claim 11, Shen teaches, from fig. 1 and figure A above, the said semiconductor device wherein the first semiconductor package (C) comprises a ball (5) grid array with the first semiconductor chip (2c) (see fig. 1 and fig.4), flip-chip mounted on the first carrier substrate (1c), and the second semiconductor package (B) comprises any of a ball (5) grid array and a chip-size package, in which the second semiconductor chip (2b) mounted on the

second carrier substrate (1b) is mold-sealed (23).

16. With respect to claim 12, Shen teaches, from figs 1 and 5 and figure A above, an electronic device, comprising:

a first carrier substrate (1b), in which a plurality of first joining points are formed, the first joining points including different areas for protruding electrodes (3 and 5);

a first electronic component (2b), flip-chip mounted on the first carrier substrate (1b);

a second carrier substrate (1c), in which a plurality of second joining points are formed, the second joining points including different areas for the protruding electrodes (3 and 5) and being arranged so as to be opposed to the first joining points;

a second electronic component (2c), mounted on the second carrier substrate (1c); and a sealing material (23) sealing the second electronic component. (Note that the joining points of the electrodes 3 and 5 have different contact areas on the substrates).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (US Patent No. 6,774,473) as applied to claim 1 above, and further in view of Chandran (US Patent No. 6,750,549).

19. Shen teaches the semiconductor device with two stacked packages as described above.

20. However Shen does not teach that as an interval between the first semiconductor package and the second semiconductor package becomes larger, the areas of the first joining points and the areas of the second joining points gradually become smaller.

21. Chandran does teach, from fig. 3, a semiconductor device wherein as an interval between a first semiconductor package (300) and a second semiconductor package (not shown but joined along line 360) becomes larger, the areas of the first joining points and the areas of the second joining points gradually become smaller.

22. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the stacked device of Shen utilizing the different joining areas in order to increase the co-planarity of the contact array and thereby improving device connection reliability. (see column 2, lines 9-18)

23. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byun as applied to claim 7 above, and further in view of Hamaguchi (US Patent No. 6,633,078).

24. Byun teaches the semiconductor device as stated above.

25. However Byun does not teach that as an interval between the first semiconductor package and the second semiconductor package becomes larger, the volumes of the protruding electrodes gradually become larger.

26. Hamaguchi does teach, from fig. 7B, a semiconductor device wherein as an interval between a first semiconductor package and a mounting board becomes larger, the volumes of the protruding electrodes gradually become larger.

27. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create Byun's device utilizing Hamaguchi's feature of volumetric increasing electrodes in order to further account for substrate or chip warping and provide better connection reliability. (see column 3, lines 12-30 of 6,633,078)

28. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (US Patent No. 6,774,473) in view of Hamaguchi (US Patent No. 6,633,078).

29. With respect to claim 13, Shen teaches, from figs 1 and 5 and figure A above, an electronic device, comprising:

a first carrier substrate (1c);

a first electronic component (2c), flip-chip mounted on the first carrier substrate (1c);

a second carrier substrate (1b), mounted on the first carrier substrate (2b) through a plurality of protruding electrodes (3), so as to be held above the first electronic component (2c);

a second electronic component (2b), mounted on the second carrier substrate (1b); and

a sealing material (23) sealing the second electronic component.

30. However, Shen does not teach the plurality of electrodes including different volumes.

31. Hamaguchi does teach, from fig. 7B, a semiconductor device wherein as an interval between a first semiconductor package and a mounting board becomes larger, the volumes of the protruding electrodes gradually become larger.

32. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create Shen's device utilizing Hamaguchi's feature of volumetric increasing electrodes in order to further account for substrate or chip warping and provide better connection reliability. (see column 3, lines 12-30 of 6,633,078)

With respect to claim 16, Shen teaches an electronic apparatus comprising:

a first semiconductor package (C);

a second semiconductor package (B), stacked on the first semiconductor package (C) through a plurality of protruding electrodes (3);

and a motherboard (See column 4, lines 43-47), on which the first semiconductor package (C) is mounted.

33. However, Shen does not teach the plurality of electrodes including different volumes.

34. Hamaguchi does teach, from fig. 7B, a semiconductor device wherein as an interval between a first semiconductor package and a mounting board becomes larger, the volumes of the protruding electrodes gradually become larger.

35. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create Shen's device utilizing Hamaguchi's feature of volumetric increasing electrodes in order to further account for substrate or chip warping and provide better connection reliability. (see column 3, lines 12-30 of 6,633,078)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
9/28/2005

ANH D. MAI
PRIMARY EXAMINER